NB7VQ1006M

1.8V / 2.5V 10Gbps Equalizer Receiver with 1:6 Differential CML Outputs

Multi−Level Inputs w/ Internal Termination

ON Semiconductor®

http://onsemi.com

Description

The NB7VQ1006M is a high performance EQualizer Receiver (signal enhancer) that operates up to 10 Gbps/7.5 GHz with a 1.8 V or 2.5 V power supply. When placed in series with a Data/Clock path, it will enhance the degraded signal transmitted across a FR4 backplane or cable interconnect and output six identical CML copies of the input signal.

The EQualizer ENable pin (EQEN) allows the IN/$\overline{IN}$ inputs to either flow through or bypass the EQualizer section. Control of the EQualizer function is realized by setting EQEN; When EQEN is set Low, the IN / $\overline{IN}$ inputs bypass the Equalizer. When EQEN is set High, the IN / $\overline{IN}$ inputs flow through the EQualizer. The default state at start−up is LOW.

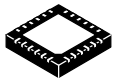
The differential Data/Clock inputs incorporate a pair of internal 50 Ω Termination resistors, in a 100 Ω center−tapped configuration, via the VT Pin and will accept differential LVPECL, CML or LVDS logic levels. This feature provides transmission line termination on−chip, at the receiver end, eliminating external components.

The NB7VQ1006M is a member of the PEEQ GigaComm™ family of high performance Data/Clock products.

Features

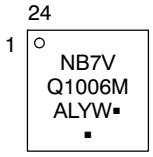
- Maximum Input Data Rate > 10 Gbps
- Maximum Input Clock Frequency > 7.5 GHz
- Backplane and Cable Interconnect Compensation
- 225 ps Typical Propagation Delay
- 30 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak−to−Peak, Typical
- Operating Range: V_{CC} = 1.71 V to 2.625 V, GND = 0 V
- Internal Input Termination Resistors, 50 Ω
- QFN−24 Package, 4 mm x 4 mm
- −40°C to +85°C Ambient Operating Temperature
- These are Pb−Free Devices*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



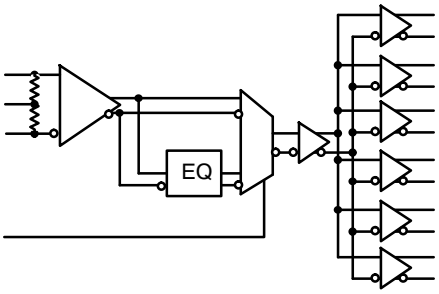
QFN−24
MN SUFFIX
CASE 485L

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.



SIMPLIFIED BLOCK DIAGRAM

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

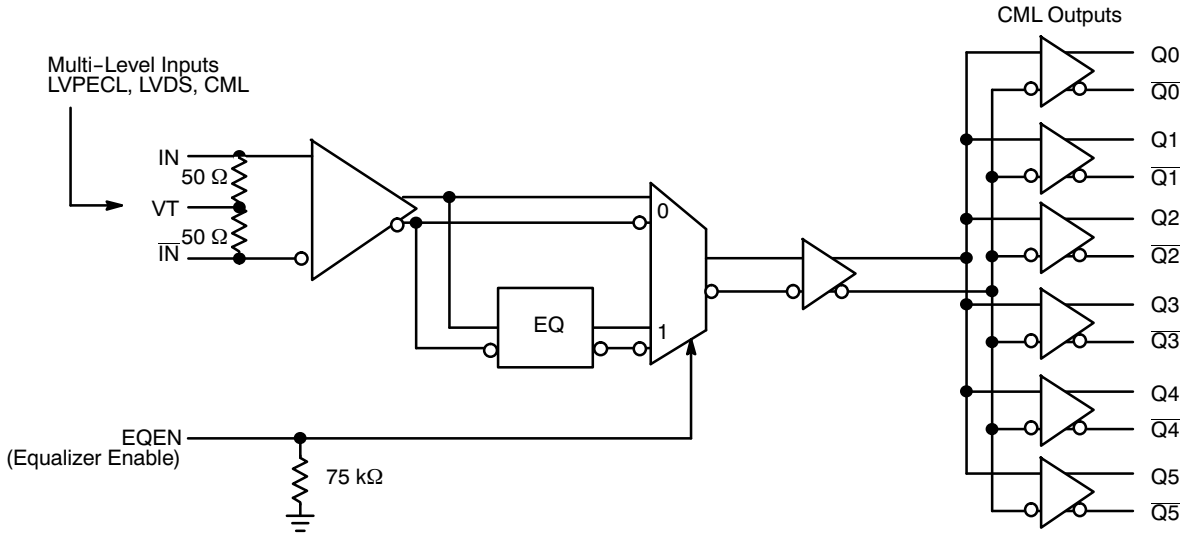


Figure 1. Detailed Block Diagram of NB7VQ1006M

Table 1. EQUALIZER ENABLE FUNCTION

EQEN	Function
0	IN/$\overline{IN}$ Inputs Bypass the EQualizer Section
1	Inputs Flow through the EQualizer

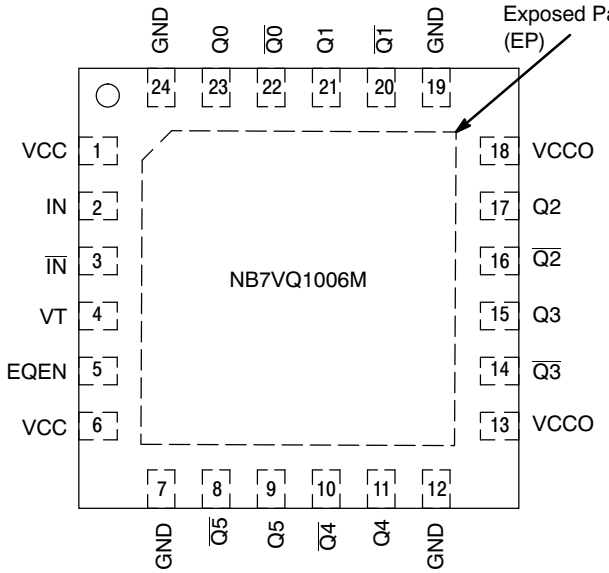


Figure 2. QFN−24 Lead Pinout (Top View)

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	VCC		Positive Supply Voltage for the Core Logic
2	IN	LVPECL, CML, LVDS Input	Non−inverted Differential Clock/Data Input. (Note 1)
3	$\overline{IN}$	LVPECL, CML, LVDS Input	Inverted Differential Clock/Data Input. (Note 1)
4	VT		Internal 50 Ω Termination Pin for IN and $\overline{IN}$
5	EQEN	LVCMOS Input	Equalizer Enable Input; pin will default LOW when left open (has internal pull−down resistor)
6	VCC		Positive Supply Voltage for the Core Logic
7	GND		Negative Supply Voltage
8	$\overline{Q5}$	CML	Inverted Differential Output. (Note 1)
9	Q5	CML	Non−inverted Differential Output. (Note 1)
10	$\overline{Q4}$	CML	Inverted Differential Output. (Note 1)
11	Q4	CML	Non−inverted Differential Output. (Note 1)
12	GND		Negative Supply Voltage
13	VCCO		Positive Supply Voltage for the pre−amplifier and output buffer
14	$\overline{Q3}$	CML	Inverted Differential Output. (Note 1)
15	Q3	CML	Non−inverted Differential Output. (Note 1)
16	$\overline{Q2}$	CML	Inverted Differential Output. (Note 1)
17	Q2	CML	Non−inverted Differential Output. (Note 1)
18	VCCO		Positive Supply Voltage for the pre−amplifier and output buffer
19	GND		Negative Supply Voltage
20	$\overline{Q1}$	CML	Inverted Differential Output. (Note 1)
21	Q1	CML	Non−inverted Differential Output. (Note 1)
22	$\overline{Q0}$	CML	Inverted Differential Output. (Note 1)
23	Q0	CML	Non−inverted Differential Output. (Note 1)
24	GND		Negative Supply Voltage
−	EP	−	The Exposed Pad (EP) on the QFN−24 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to GND and is recommended to be electrically connected to GND on the PC board.

1. In the differential configuration when the input termination pin (VT) is connected to a common termination voltage or left open, and if no signal is applied on IN/$\overline{IN}$, then the device will be susceptible to self−oscillation. Qn/$\overline{Qn}$ outputs have internal 50 Ω source.
2. All VCC, VCCO and GND pins must be externally connected to the same power supply voltage to guarantee proper device operation.

Table 3. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 4 kV > 200 V
Moisture Sensitivity (Note 3)		Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		244
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

3. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}, V_{CCO}	Positive Power Supply	GND = 0 V		3.0	V
V_I	Input Voltage	GND = 0 V		−0.5 to V_{CC} + 0.5	V
V_{INPP}	Differential Input Voltage |D − $\overline{D}$|			V_{CC} − GND	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)			±40	mA
I_{OUT}	Output Current Through R_T (50 Ω Resistor)			±40	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 4) TGSD 51−6 (2S2P Multilayer Test Board) with Filled Thermal Vias	0 lfpm 500 lfpm	QFN−24 QFN−24	37 32	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	Standard Board	QFN−24	11	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS – CML OUTPUT V_{CC} = V_{CCO} = 1.71 V to 2.625 V; GND = 0 V T_A = −40°C to 85°C

Symbol	Characteristic		Min	Typ	Max	Unit
POWER SUPPLY CURRENT (Inputs and Outputs open)						
I_{CC}	Power Supply Current, Core Logic	V_{CC} = 2.5V		100	115	mA
		V_{CC} = 1.8V		85	95	
I_{CCO}	Power Supply Current, Outputs	V_{CC} = 2.5V		180	200	
		V_{CC} = 1.8V		150	175	
CML OUTPUTS (Notes 5 and 6) (Figure 10)						
V_{OH}	Output HIGH Voltage		V_{CC} – 40	V_{CC} – 10	V_{CC}	mV
		V_{CC} = 2.5 V	2460	2490	2500	
		V_{CC} = 1.8 V	1760	1790	1800	
V_{OL}	Output LOW Voltage		V_{CC} – 600	V_{CC} – 500	V_{CC} – 400	mV
		V_{CC} = 2.5V	1900	2000	2100	
		V_{CC} = 1.8V	V_{CC} – 525	V_{CC} – 425	V_{CC} – 300	
			1275	1375	1500	
DATA/CLOCK INPUTS (IN, $\overline{IN}$) (Note 7) (Figures 6 & 7)						
V_{IHD}	Differential Input HIGH Voltage		1100		V_{CC}	mV
V_{ILD}	Differential Input LOW Voltage		GND		V_{CC} – 100	mV
V_{ID}	Differential Input Voltage (V_{IHD} – V_{ILD})		100		1200	mV
I_{IH}	Input HIGH Current		−150	30	+150	μA
I_{IL}	Input LOW Current		−150	−40	+150	μA
CONTROL INPUTS (EQEN)						
V_{IH}	Input HIGH Voltage		V_{CC} x 0.65		V_{CC}	mV
V_{IL}	Input LOW Voltage		GND		V_{CC} x 0.35	mV
I_{IH}	Input HIGH Current		−150	25	+150	μA
I_{IL}	Input LOW Current		−150	10	+150	μA
TERMINATION RESISTORS						
R_{TIN}	Internal Input Termination Resistor		40	50	60	Ω
R_{TOUT}	Internal Output Termination Resistor		40	50	60	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

5. CML outputs loaded with 50 Ω to V_{CC} for proper operation.
6. Input and output parameters vary 1:1 with V_{CC}/V_{CCO}.
7. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.

Table 6. AC CHARACTERISTICS V_{CC} = V_{CCO} = 1.71 V to 2.625 V; GND = 0 V T_A = −40°C to 85°C (Note 8)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{DATA}	Maximum Operating Input Data Rate	10			Gbps
f_{INCLK}	Maximum Input Clock Frequency V_{CC} = 2.5V V_{CC} = 1.8V	7.5 6.5			GHz
V_{OUTPP}	Output Voltage Amplitude EQEN = 0 or 1 $f_{in} \le$ 5.0 GHz V_{CC} = 2.5V (See Figures 4, Note 9) $f_{in} \le$ 7.5 GHz V_{CC} = 2.5V $f_{in} \le$ 5 GHz V_{CC} = 1.8V $f_{in} \le$ 6.5 GHz V_{CC} = 1.8V	275 225 225 200	440 360 360 315		mV
V_{CMR}	Input Common Mode Range (Differential Configuration, Note 10) (Figure 8)	1050		V_{CC} − 50	mV
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential, IN/$\overline{IN}$ to Q/$\overline{Q}$	170	225	315	ps
t_{PLH} TC	Propagation Delay Temperature Coefficient −40°C to +85°C		30		fs/°C
t_{DC}	Output Clock Duty Cycle	48	50	52	%
t_{SKEW}	Duty Cycle Skew (Note 11) Within Device Skew (Note 12) Device to Device Skew (Note 13)		0.15 10 20	1 25 40	ps
t_{JITTER}	Clock Jitter RMS, 1000 cycles (Note 14) EQEN = 1 $f_{in} \le$ 5.0 GHz 5 GHz $\le f_{in} \le$ 7.5 GHz Data Dependent Jitter (DDJ) (Note 15) EQEN = 1, ≤10 Gbps V_{CC} = 2.5 V V_{CC} = 1.8 V		0.2 0.2 3 3	0.7 1.2 40 20	ps
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 16) (Figure 6)	100		1200	mV
t_r, t_f	Output Rise/Fall Times Q, $\overline{Q}$, (20% − 80%)		30	65	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

8. Measured using a 400 mV source, 50% duty cycle 1GHz clock source. All outputs must be loaded with external 50 Ω to V_{CC}. Input edge rates 40 ps (20% − 80%).
9. Output voltage swing is a single−ended measurement operating in differential mode.
10. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC}. The V_{CMR} range is referenced to the most positive side of the differential input signal.
11. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw}− and T_{pw}+ @ 5 GHz.
12. Within device skew compares coincident edges.
13. Device to device skew is measured between outputs under identical transition
14. Additive CLOCK jitter with 50% duty cycle clock signal.
15. Additive Peak−to−Peak jitter with input NRZ data at PRBS23.
16. Input voltage swing is a single−ended measurement operating in differential mode, with minimum propagation change of 25 ps.

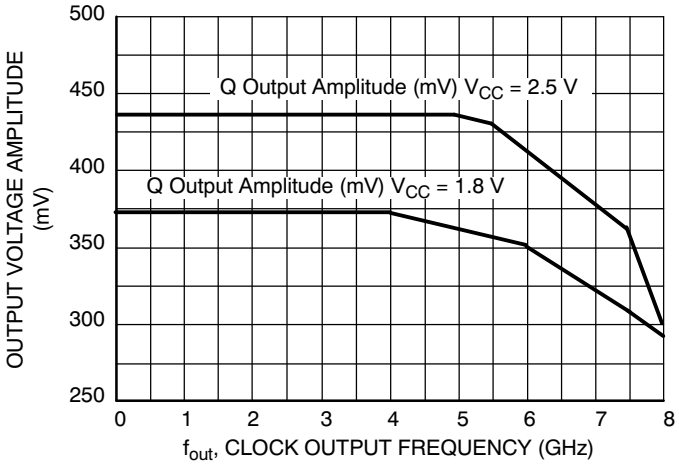


Figure 3. Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typ), EQEN = 0 or 1

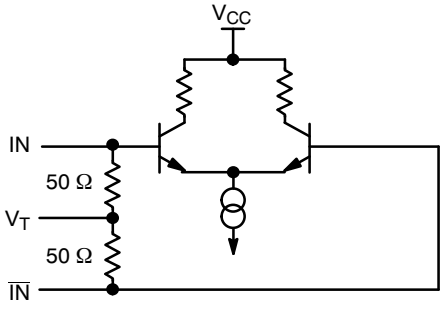


Figure 4. Input Structure

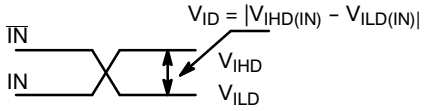


Figure 5. Differential Inputs Driven Differentially

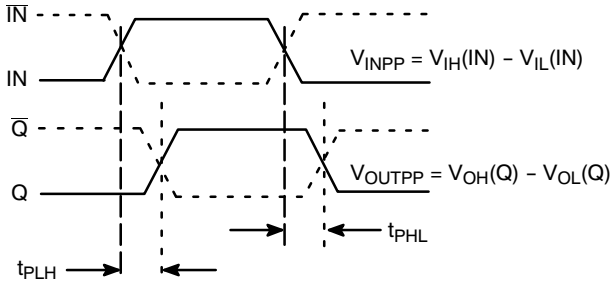


Figure 6. AC Reference Measurement

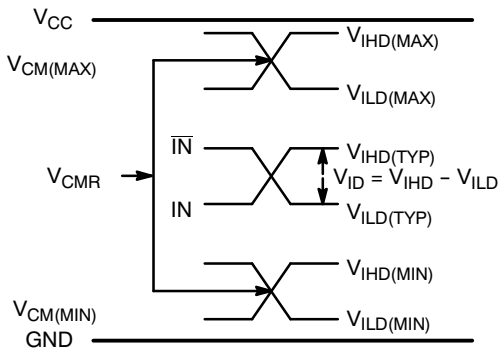


Figure 7. V_{CMR} Diagram

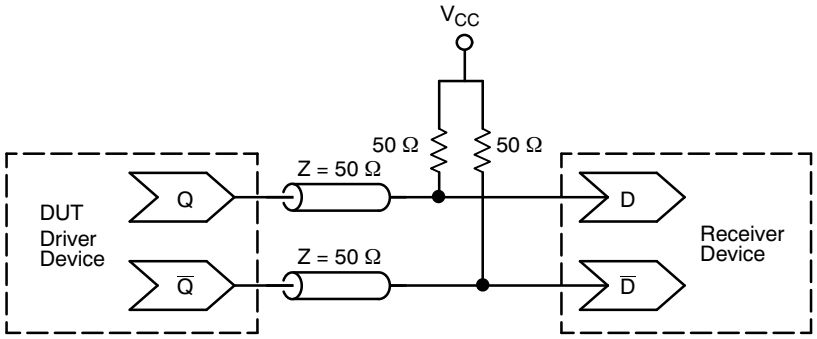


Figure 8. Typical Termination for CML Output Driver and Device Evaluation

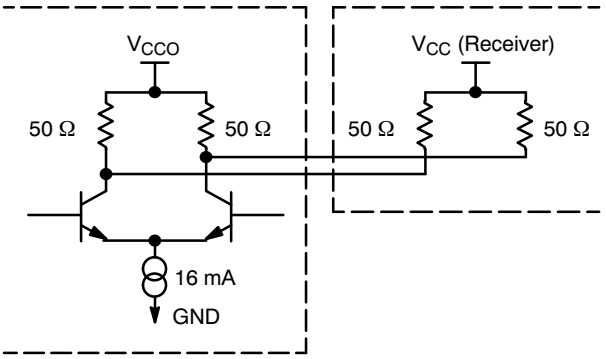


Figure 9. Typical CML Output Structure and Termination

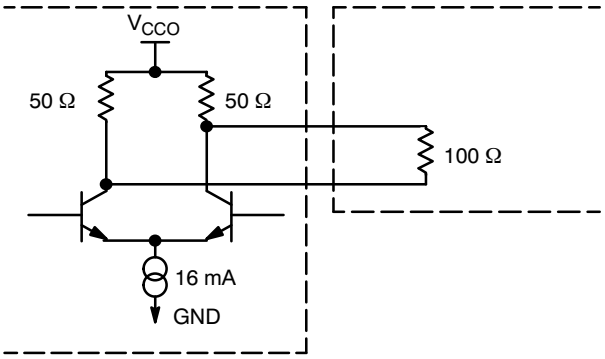


Figure 10. Alternative Output Termination

APPLICATION INFORMATION

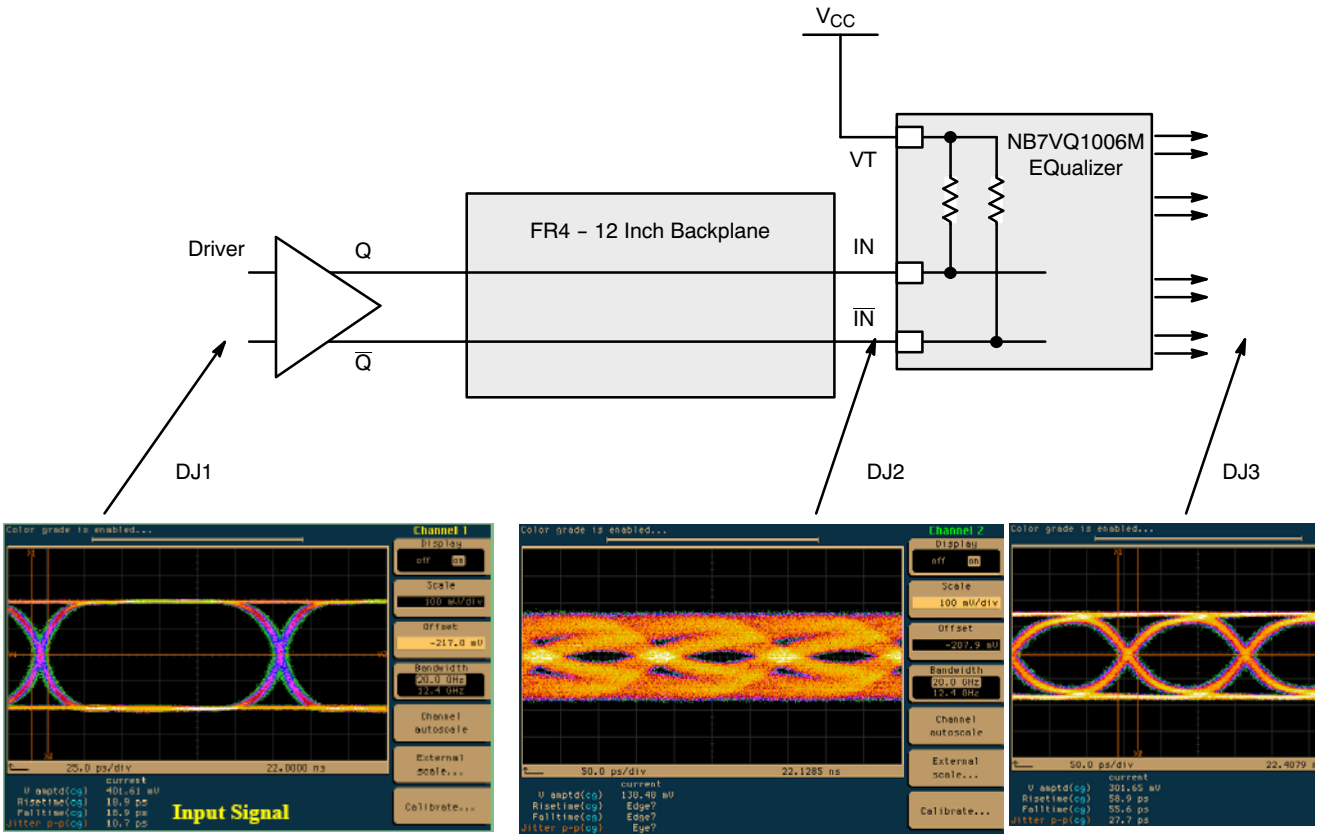


Figure 11. Typical NB7VQ1006 Equalizer Application and Interconnect with PRBS23 pattern at 6.5 Gbps

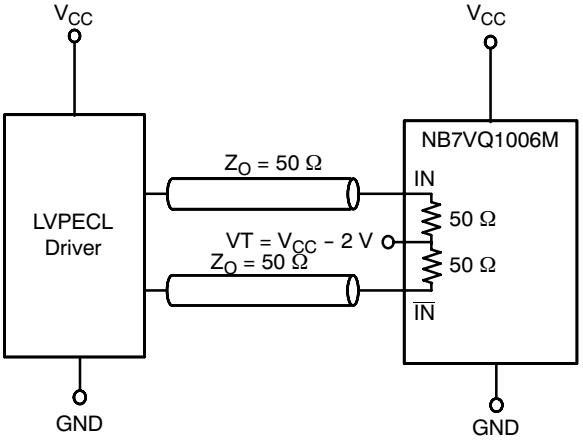


Figure 12. LVPECL Interface

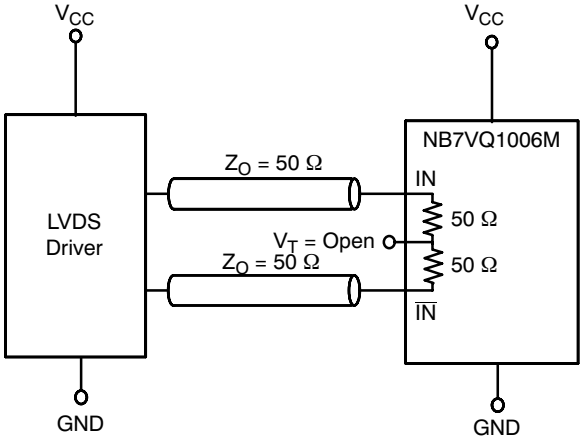


Figure 13. LVDS Interface

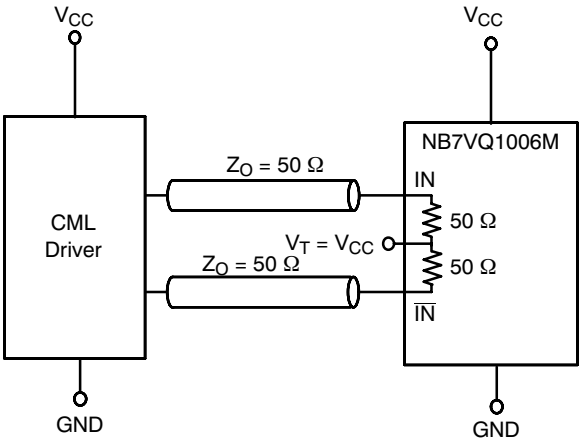


Figure 14. Standard 50 Ω Load CML Interface

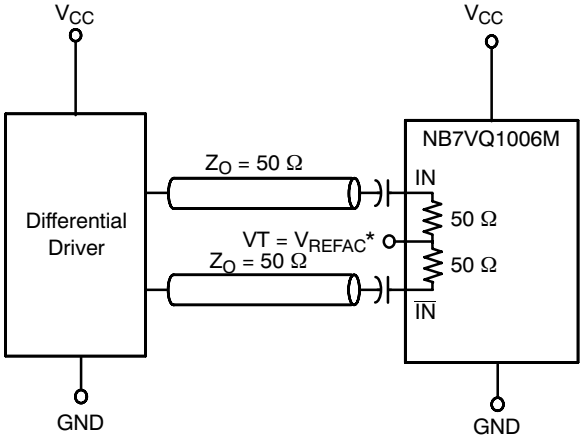


Figure 15. Capacitor−Coupled Differential Interface (VT Connected to External V_{REFAC})

*V_{REFAC} bypassed to ground with a 0.01 μF capacitor

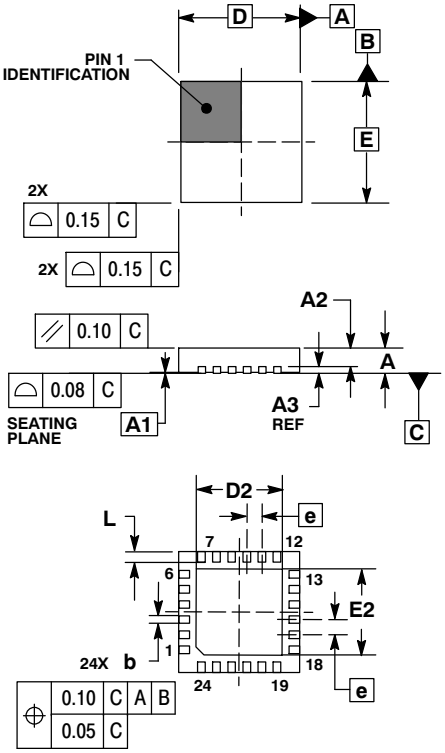
ORDERING INFORMATION

Device	Package	Shipping†
NB7VQ1006MMNG	QFN−24 (Pb−Free)	92 Units / Rail
NB7VQ1006MMNHTBG	QFN−24 (Pb−Free)	100 / Tape & Reel
NB7VQ1006MMNTXG	QFN−24 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

QFN 24
MN SUFFIX
24 PIN QFN, 4x4
CASE 485L−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.23	0.28
D	4.00 BSC	
D2	2.70	2.90
E	4.00 BSC	
E2	2.70	2.90
e	0.50 BSC	
L	0.35	0.45

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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